	L #	Hits	Search Text	DBs
1	L1	59740	(bit field tag flag cod$3 encod$3) near10 instruction	USPAT; US-PGPUB
2	L12	24001	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer locat$3 position) near10 (call$3 different separate$3 first second subroutine above below minus plus subtract$3 add$3))	USPAT; US-PGPUB
3	L13	399	1 near99 12	USPAT; US-PGPUB
4	L14	11017	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer) near10 (call$3 different separate$3 second subroutine above below minus plus subtract$3 add$3))	USPAT; US-PGPUB
5	L16	235	13 not 15	USPAT; US-PGPUB
6	L15	164	1 near99 14	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040025150 A1	☐	Compiler, compiler apparatus and compilation method	717/154
2	US 20030188137 A1	☒	Parallel subword instructions with distributed results	712/221
3	US 20030154358 A1	☒	Apparatus and method for dispatching very long instruction word having variable length	712/24
4	US 20030135848 A1	☒	Use of multiple procedure entry and/or exit points to improve instruction scheduling	717/158
5	US 20030126410 A1	☒	System and method of reducing the number of copies from alias registers to real registers in the commitment of instructions	712/218
6	US 20030115579 A1	☒	Optimizing source code for iterative execution	717/152
7	US 20030061499 A1	☒	Data encryption and decryption	713/189
8	US 20030033504 A1	☒	Micro-controller for reading out compressed instruction code and program memory for compressing instruction code and storing therein	712/210
9	US 20030033482 A1	☒	Micro-controller for reading out compressed instruction code and program memory for compressing instruction code and storing therein	711/119
10	US 20030023837 A1	☒	Register file backup queue	712/228
11	US 20030005268 A1	☒	Find first bit value instruction	712/223
12	US 20020196678 A1	☒	Eliminating store/restores within hot function prolog/epilogs using volatile regosters	365/200
13	US 20020169969 A1	☒	Information processing unit having tamper - resistant system	713/190
14	US 20020147901 A1	☒	Method of handling instructions within a processor with decoupled architecture, in particular a processor for digital signal processing, and corresponding processor	712/225
15	US 20020144084 A1	☒	Processor for executing highly efficient VLIW	712/24
16	US 20020138715 A1	☒	Microprocessor executing data transfer between memory and register and data transfer between registers in response to single push/pop instruction	712/225
17	US 20020129223 A1	☒	Processor for executing highly efficient VLIW	712/24

	Document ID	U	Title	Current OR
18	US 20020124160 A1	☒	Register file backup queue	712/228
19	US 20020124044 A1	☒	Method of handling branching instructions within a processor, in particular a processor for digital signal processing, and corresponding processor	709/200
20	US 20020087851 A1	☒	Microprocessor and an instruction converter	712/239
21	US 20020062479 A1	☒	Microcontroller with modifiable program	717/168
22	US 20020042909 A1	☒	Retargetable compiling system and method	717/149
23	US 20020032868 A1	☒	Information processing apparatus, executable module generating method, and storage medium	713/193
24	US 20020032718 A1	☒	METHOD AND APPARATUS FOR MAINTAINING TRANSLATED ROUTINE STACK IN A BINARY TRANSLATION ENVIROMENT	718/107
25	US 20020019902 A1	☒	Stack switching mechanism in a computer system	710/260
26	US 20020013893 A1	☒	Real time debugger interface for embedded systems	712/227
27	US 20020010851 A1	☒	Emulated branch effected by trampoline mechanism	712/244
28	US 20020007450 A1	☒	Line-oriented reorder buffer	712/23
29	US 6697936 B2	☒	Register file backup queue	712/228
30	US 6687857 B1	☒	Microcomputer which can execute a monitor program supplied from a debugging tool	714/38
31	US 6654878 B1	☒	Register bit scanning	712/234
32	US 6631460 B1	☒	Advanced load address table entry invalidation based on register address wraparound	712/217
33	US 6591385 B1	☒	Method and apparatus for inserting programmable latency between address and data information in a memory tester	714/718
34	US 6535903 B2	☒	Method and apparatus for maintaining translated routine stack in a binary translation environment	718/100
35	US 6512775 B1	☒	Method and apparatus for a programmable bitstream parser for audiovisual and generic decoding systems	370/428
36	US 6505296 B2	☒	Emulated branch effected by trampoline mechanism	712/244

	Document ID	U	Title	Current OR
37	US 6502237 B1	☒	Method and apparatus for performing binary translation method and apparatus for performing binary translation	717/136
38	US 6499100 B1	☒	Enhanced instruction decoding	712/210
39	US 6489963 B2	☒	Application program interface for a graphics system	345/522
40	US 6457171 B1	☒	Storage structure for dynamic management of translated code blocks in dynamic object code translation	717/138
41	US 6449736 B1	☒	Method and apparatus for providing chained breakpoints in a microprocessor	714/35
42	US 6446197 B1	☒	Two modes for executing branch instructions of different lengths and use of branch control instruction and register set loaded with target instructions	712/237
43	US 6442673 B1	☒	Update forwarding cache for address mode	712/202
44	US 6408380 B1	☒	Execution of an instruction to load two independently selected registers in a single cycle	712/225
45	US 6408375 B2	☒	System and method for register renaming	712/23
46	US 6397319 B1	☒	Process for executing highly efficient VLIW	712/24
47	US 6397235 B1	☒	Data processing device and method of computing the costine transform of a matrix	708/401
48	US 6381689 B2	☒	Line-oriented reorder buffer configured to selectively store a memory operation result in one of the plurality of reorder buffer storage locations corresponding to the executed instruction	712/215
49	US 6374347 B1	☒	Register file backup queue	712/228
50	US 6360309 B1	☒	System and method for assigning tags to control instruction processing in a superscalar processor	712/23
51	US 6321331 B1	☒	Real time debugger interface for embedded systems	712/244
52	US 6282633 B1	☒	High data density RISC processor	712/208
53	US 6272617 B1	☒	System and method for register renaming	712/23
54	US 6260190 B1	☒	Unified compiler framework for control and data speculation with recovery code	717/156
55	US 6250821 B1	☒	Method and apparatus for processing branch instructions in an instruction buffer	712/238
56	US 6249862 B1	☒	Dependency table for reducing dependency checking hardware	712/218
57	US 6247120 B1	☒	Instruction buffer for issuing instruction sets to an instruction decoder	712/238
58	US 6240544 B1	☒	Simulation system, simulation evaluation system, simulation method, and computer-readable memory containing a simulation program, having less trace information for reverse execution	717/135

	Document ID	U	Title	Current OR
59	US 62370 82 B1	☒	Reorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received	712/215
60	US 62267 89 B1	☒	Method and apparatus for data flow analysis	717/138
61	US 62197 79 B1	☒	Constant reconstructing processor which supports reductions in code size	712/210
62	US 62090 84 B1	☒	Dependency table for reducing dependency checking hardware	712/233
63	US 61990 95 B1	☒	System and method for achieving object method transparency in a multi-code execution environment	718/107
64	US 61957 40 B1	☒	Constant reconstructing processor that execute an instruction using an operand divided between instructions	712/24
65	US 61382 31 A	☒	System and method for register renaming	712/216
66	US 61346 51 A	☒	Reorder buffer employed in a microprocessor to store instruction results having a plurality of entries predetermined to correspond to a plurality of functional units	712/215
67	US 61287 22 A	☒	Data processing system having an apparatus for exception tracking during out-of-order operation and method therefor	712/23
68	US 61254 56 A	☒	Microcomputer with self-diagnostic unit	714/25
69	US 61087 69 A	☒	Dependency table for reducing dependency checking hardware	712/216
70	US 60918 97 A	☒	Fast translation and execution of a computer program on a non-native architecture by use of background translator	717/138
71	US 60853 06 A	☒	Processor for executing highly efficient VLIW	712/24
72	US 60617 85 A	☒	Data processing system having an apparatus for out-of-order register operations and method therefor	712/236
73	US 60264 82 A	☒	Recorder buffer and a method for allocating a fixed amount of storage for instruction results independent of a number of concurrently dispatched instructions	712/215
74	US 60095 08 A	☒	System and method for addressing plurality of data values with a single address in a multi-value store on FIFO basis	712/41
75	US 60000 28 A	☒	Means and apparatus for maintaining condition codes in an unevaluated state	712/226
76	US 59960 58 A	☒	System and method for handling software interrupts with argument passing	712/31
77	US 59872 35 A	☒	Method and apparatus for predecoding variable byte length instructions for fast scanning of instructions	712/210
78	US 59616 34 A	☒	Reorder buffer having a future file for storing speculative instruction execution results	712/218
79	US 59516 76 A	☒	Apparatus and method for direct loading of offset register during pointer load operation	712/225
80	US 59464 68 A	☒	Reorder buffer having an improved future file for storing speculative instruction execution results	712/218

	Document ID	U	Title	Current OR
81	US 5941980 A	☒	Apparatus and method for parallel decoding of variable-length instructions in a superscalar pipelined data processing system	712/204
82	US 5940859 A	☒	Emptying packed data state during execution of packed data instructions	711/147
83	US 5930509 A	☒	Method and apparatus for performing binary translation	717/159
84	US 5915110 A	☒	Branch misprediction recovery in a reorder buffer having a future file	712/239
85	US 5903741 A	☒	Method of allocating a fixed reorder buffer storage line for execution results regardless of a number of concurrently dispatched instructions	712/218
86	US 5901302 A	☒	Superscalar microprocessor having symmetrical, fixed issue positions each configured to execute a particular subset of instructions	712/215
87	US 5895492 A	☒	Processor associated blocking symbol controls for serializing the accessing of data resources in a computer system	711/147
88	US 5889947 A	☒	Apparatus and method for executing instructions that select a storage location for output values in response to an operation count	709/213
89	US 5883824 A	☒	Parallel adding and averaging circuit and method	708/445
90	US 5881216 A	☒	Register file backup queue	714/15
91	US 5878244 A	☒	Reorder buffer configured to allocate storage capable of storing results corresponding to a maximum number of concurrently receivable instructions regardless of a number of instructions received	712/218
92	US 5872951 A	☒	Reorder buffer having a future file for storing speculative instruction execution results	712/218
93	US 5870596 A	☒	Data processor allowing multifunctional instruction execution	712/225
94	US 5845307 A	☒	Auxiliary register file accessing technique	711/2
95	US 5842017 A	☒	Method and apparatus for forming a translation unit	717/158
96	US 5826053 A	☒	Speculative instruction queue and method therefor particularly suitable for variable byte-length instructions	712/210
97	US 5812836 A	☒	System for processing iterative tasks in data processing systems	712/220
98	US 5809327 A	☒	Eight-bit microcontroller having a risc architecture	712/33
99	US 5802373 A	☒	Method for providing a pipeline interpreter for a variable length instruction set	717/139
100	US 5787241 A	☒	Method and apparatus for locating exception correction routines	714/2
101	US 5778246 A	☒	Method and apparatus for efficient propagation of attribute bits in an instruction decode pipeline	712/23
102	US 5774687 A	☒	Central processing unit detecting and judging whether operation result executed by ALU in response to a first instruction code meets a predetermined condition	712/211

	Document ID	U	Title	Current OR
103	US 5768610 A	☒	Lookahead register value generator and a superscalar microprocessor employing same	712/23
104	US 5765216 A	☒	Data processor with an efficient bit move capability and method therefor	711/214
105	US 5754805 A	☒	Instruction in a data processing system utilizing extension bits and method therefor	712/200
106	US 5745780 A	☒	Method and apparatus for source lookup within a central processing unit	712/23
107	US 5742621 A	☒	Method for implementing an add-compare-select butterfly operation in a data processing system and instruction therefor	714/792
108	US 5740414 A	☒	Method and apparatus for coordinating the use of physical registers in a microprocessor	712/233
109	US 5740392 A	☒	Method and apparatus for fast decoding of 00H and OFH mapped instructions	712/210
110	US 5727194 A	☒	Repeat-bit based, compact system and method for implementing zero-overhead loops	712/241
111	US 5706466 A	☒	Von Neumann system with harvard processor and instruction buffer	711/125
112	US 5699460 A	☒	Image compression coprocessor with data flow control and multiple processing units	382/307
113	US 5666519 A	☒	Method and apparatus for detecting and executing cross-domain calls in a computer system	703/23
114	US 5634119 A	☒	Computer processing unit employing a separate millicode branch history table	712/240
115	US 5625784 A	☒	Variable length instructions packed in a fixed length double instruction	712/210
116	US 5611062 A	☒	Specialized millicode instruction for string operations	712/200
117	US 5588113 A	☒	Register file backup queue	714/15
118	US 5574925 A	☒	Asynchronous pipeline having condition detection among stages in the pipeline	712/25
119	US 5564057 A	☒	Microprocessor architecture which facilitates input/output utilizing pairs of registers which the same address	712/38
120	US 5560029 A	☒	Data processing system with synchronization coprocessor for multiple threads	712/25
121	US 5544244 A	☒	Method for protecting an enciphered computer object code against cryptanalysis	713/190
122	US 5497456 A	☒	Apparatus for transferring information between an interrupt producer and an interrupt service environment	714/29
123	US 5487159 A	☒	System for processing shift, mask, and merge operations in one instruction	712/223
124	US 5455955 A	☒	Data processing system with device for arranging instructions	712/208
125	US 5442704 A	☒	Secure memory card with programmed controlled security access control	711/163

	Document ID	U	Title	Current OR
126	US 5430850 A	☒	Data processing system with synchronization coprocessor for multiple threads	719/314
127	US 5421029 A	☒	Multiprocessor including system for pipeline processing of multi-functional instructions	712/225
128	US 5406644 A	☒	Apparatus and method for emulating a computer instruction set using a jump table in the host computer	703/23
129	US 5398330 A	☒	Register file backup queue	714/15
130	US 5390307 A	☒	Apparatus for a multi-data store or load instruction for transferring multiple contiguous storage locations in one transfer operation	712/225
131	US 5390135 A	☒	Parallel shift and add circuit and method	708/518
132	US 5386580 A	☒	Data processor	712/32
133	US 5363322 A	☒	Data processor with an integer multiplication function on a fractional multiplier	708/620
134	US 5355465 A	☒	Data storing device having a plurality of registers allotted for one address	711/200
135	US 5349681 A	☒	Bit searching circuit and data processor including the same	712/227
136	US 5345569 A	☒	Apparatus and method for resolving dependencies among a plurality of instructions within a storage device	712/217
137	US 5321821 A	☒	System for processing parameters in instructions of different format to execute the instructions using same microinstructions	712/210
138	US 5287475 A	☒	Data processing apparatus operable in extended or unextended virtual address spaces without software modification	711/2
139	US 5253349 A	☒	Decreasing processing time for type 1 dyadic instructions	712/223
140	US 5233693 A	☒	First-in first-out storage facility having bypassing loop thereof	712/218
141	US 5179689 A	☒	Dataprocessing device with instruction cache	710/22
142	US 5081574 A	☒	Branch control in a three phase pipelined signal processor	712/234
143	US 5077659 A	☒	Data processor employing the same microprograms for data having different bit lengths	712/210
144	US 5032980 A	☒	Information processing system with instruction address saving function corresponding to priority levels of interruption information	712/228
145	US 5001753 A	☒	Crytographic system and process and its application	380/29
146	US 4992938 A	☒	Instruction control mechanism for a computing system with register renaming, map table and queues indicating available registers	712/217
147	US 4991078 A	☒	Apparatus and method for a pipelined central processing unit in a data processing system	712/218
148	US 4969091 A	☒	Apparatus for stack control employing mixed hardware registers and memory	712/228

	Document ID	U	Title	Current OR
149	US 4951193 A	☒	Parallel computer with distributed shared memories and distributed task activating circuits	711/206
150	US 4947315 A	☒	System for controlling instrument using a levels data structure and concurrently running compiler task and operator task	717/111
151	US 4943915 A	☒	Apparatus and method for synchronization of a coprocessor unit in a pipelined central processing unit	712/34
152	US 4896258 A	☒	Data processor provided with instructions which refer to both tagged and tagless data	712/236
153	US 4896133 A	☒	Parallel string processor and method for a minicomputer	340/146.2
154	US 4884414 A	☒	Adaptive defrost system	62/156
155	US 4794517 A	☒	Three phased pipelined signal processor	712/32
156	US 4777587 A	☒	System for processing single-cycle branch instruction in a pipeline having relative, absolute, indirect and trap addresses	712/235
157	US 4771376 A	☒	Processor	703/27
158	US 4768149 A	☒	System for managing a plurality of shared interrupt handlers in a linked-list data structure	710/47
159	US 4763255 A	☒	Method for generating short form instructions in an optimizing compiler	717/153
160	US 4761731 A	☒	Look-ahead instruction fetch control for a cache memory	711/156
161	US 4760608 A	☒	Image processing method and apparatus	382/295
162	US 4704678 A	☒	Function set for a microcomputer	718/106
163	US 4654817 A	☒	Real time controller	712/208
164	US 4597044 A	☒	Apparatus and method for providing a composite descriptor in a data processing system	713/100
165	US 4574349 A	☒	Apparatus for addressing a larger number of instruction addressable central processor registers than can be identified by a program instruction	711/154
166	US 4542476 A	☒	Arithmetic logic unit	708/518
167	US 4535404 A	☒	Method and apparatus for addressing a peripheral interface by mapping into memory address space	710/59
168	US 4525776 A	☒	Arithmetic logic unit arranged for manipulating bits	712/221
169	US 4506325 A	☒	Reflexive utilization of descriptors to reconstitute computer instructions which are Huffman-like encoded	341/65
170	US 4497022 A	☒	Method and apparatus for measurements of channel operation	714/47
171	US 4482968 A	☒	Method and apparatus for robot control	318/568.22

	Document ID	U	Title	Current OR
172	US 4459661 A	☒	Channel address control system for a virtual machine system	718/100
173	US 4454580 A	☒	Program call method and call instruction execution apparatus	712/242
174	US 4430711 A	☒	Central processing unit	711/215
175	US 4419739 A	☒	Decentralized generation of synchronized clock control signals having dynamically selectable periods	713/600
176	US 4410956 A	☒	Exponential operation device	708/605
177	US 4398245 A	☒	Data processing system having an instruction pipeline for processing a transfer instruction	711/214
178	US 4398243 A	☒	Data processing system having a unique instruction processor system	712/211
179	US 4388685 A	☒	Central processor with apparatus for extended virtual addressing	711/2
180	US 4388682 A	☒	Microprogrammable instruction translator	712/211
181	US 4378589 A	☒	Undirectional looped bus microcomputer architecture	712/2
182	US 4370731 A	☒	System for entering temperature control data and displaying it with the temperature scale	219/506
183	US 4339793 A	☒	Function integrated, shared ALU processor apparatus and method	712/32
184	US 4337510 A	☒	Read control system for a control storage device	712/211
185	US 4314331 A	☒	Cache unit information replacement apparatus	711/133
186	US 4312036 A	☒	Instruction buffer apparatus of a cache unit	711/3
187	US 4309756 A	☒	Method of automatically evaluating source language logic condition sets and of compiling machine executable instructions directly therefrom	717/155
188	US 4298927 A	☒	Computer instruction prefetch circuit	712/207
189	US 4293907 A	☒	Data processing apparatus having op-code extension register	712/208
190	US 4281416 A	☒	Light source system in an optical transmission repeater	398/178
191	US 4245304 A	☒	Cache arrangement utilizing a split cycle mode of operation	711/122
192	US 4208716 A	☒	Cache arrangement for performing simultaneous read/write operations	711/3
193	US 4181934 A	☒	Microprocessor architecture with integrated interrupts and cycle steals prioritized channel	710/40

	Document ID	U	Title	Current OR
194	US 4172284 A	☒	Priority interrupt apparatus employing a plural stage shift register having separate interrupt mechanisms coupled to the different stages thereof for segregating interrupt requests according to priority levels	710/264
195	US 4167779 A	☒	Diagnostic apparatus in a data processing system	712/212
196	US 4156279 A	☒	Microprogrammed data processing unit including a multifunction secondary control store	712/209
197	US 4130869 A	☒	Microprogram controlled system	712/208
198	US 4126896 A	☒	Microprogrammed large-scale integration (LSI) microprocessor	712/208
199	US 4124891 A	☒	Memory access system	711/100
200	US 4115866 A	☒	Data processing network for communications switching system	379/222

	L #	Hits	Search Text	DBs
1	L1	59740	(bit field tag flag cod$3 encod$3) near10 instruction	USPAT; US-PGPUB
2	L12	24001	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer locat$3 position) near10 (call$3 different separate$3 first second subroutine above below minus plus subtract$3 add$3))	USPAT; US-PGPUB
3	L13	399	1 near99 12	USPAT; US-PGPUB
4	L14	11017	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer) near10 (call$3 different separate$3 second subroutine above below minus plus subtract$3 add$3))	USPAT; US-PGPUB
5	L15	164	1 near99 14	USPAT; US-PGPUB
6	L16	235	13 not 15	USPAT; US-PGPUB

	Document ID	U	Title	Current OR
1	US 20040064682 A1	☐	System and method for simultaneously executing multiple conditional execution instruction groups	712/226
2	US 20040059895 A1	☒	Microprocessor circuit for portable data carriers and method for operating the circuit	712/223
3	US 20040034858 A1	☒	Programming a multi-threaded processor	718/108
4	US 20040019817 A1	☒	Method and apparatus for imaging device and timing generator	713/400
5	US 20040015927 A1	☒	Percolating hot function store/restores to colder calling functions	717/155
6	US 20040006687 A1	☒	Processor and instruction control method	712/220
7	US 20030233386 A1	☒	High speed virtual machine and compiler	718/100
8	US 20030217199 A1	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/1
9	US 20030191792 A1	☒	High speed virtual machine and compiler	718/100
10	US 20030188128 A1	☒	Executing stack-based instructions within a data processing apparatus arranged to apply operations to data items stored in registers	712/202
11	US 20030142355 A1	☒	Image processing method and image forming apparatus	358/2.1
12	US 20030141434 A1	☒	Semiconductor integrated circuit device having a plurality of photo detectors and processing elements	250/208.1
13	US 20030140338 A1	☒	Method, apparatus and article for generation of debugging information	717/162
14	US 20030123744 A1	☒	Multi-resolution image data management system and method based on tiled wavelet-like transform and sparse data coding	382/240
15	US 20030051087 A1	☒	Interrupt handlers used in different modes of operations	710/260
16	US 20020194459 A1	☒	Method and apparatus for saving and restoring processor register values and allocating and deallocating stack memory	712/228
17	US 20020184472 A1	☒	Microcomputer	712/33

	Document ID	U	Title	Current OR
18	US 20020161988 A1	☒	Data processing circuits and interfaces	712/221
19	US 20020054612 A1	☒	Integrated circuit configurations and methods for providing functions for public telephones	370/535
20	US 20020032891 A1	☒	Data processing system and data processing method	714/766
21	US 20020002665 A1	☒	"STACK ORIENTED DATA PROCESSING DEVICE "	712/202
22	US 20010044866 A1	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/305
23	US 20010010072 A1	☒	Instruction translator translating non-native instructions for a processor into native instructions therefor, instruction memory with such translator, and data processing apparatus using them	712/209
24	US 20010010071 A1	☒	Stack oriented data processing device	712/11
25	US 20010001328 A1	☒	Link apparatus and virtual machine	717/141
26	US 6715142 B1	☒	Execution program generation method, execution program generation apparatus, execution program execution method, and computer-readable storage medium	717/159
27	US 6675297 B1	☒	Method and apparatus for generating and using a tamper-resistant encryption key	713/190
28	US 6665793 B1	☒	Method and apparatus for managing access to out-of-frame Registers	712/228
29	US 6615300 B1	☒	Fast look-up of indirect branch destination in a dynamic translation system	710/100
30	US 6587910 B2	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/306
31	US 6557093 B2	☒	Stack oriented data processing device	712/202
32	US 6502183 B2	☒	Stack oriented data processing device	712/202
33	US 6480940 B1	☒	Method of controlling cache memory in multiprocessor system and the multiprocessor system based on detection of predetermined software module	711/141
34	US 6467082 B1	☒	Methods and apparatus for simulating external linkage points and control transfers in source translation systems	717/127
35	US 6463524 B1	☒	Superscalar processor and method for incrementally issuing store instructions	712/221
36	US 6434690 B1	☒	Microprocessor having a DSP and a CPU and a decoder discriminating between DSP-type instructions and CUP-type instructions	712/35
37	US 6425047 B1	☒	Process containing address decoders suited to improvements in clock speed	711/101

	Document ID	U	Title	Current OR
38	US 6408385 B1	☒	Data processor	712/243
39	US 6405311 B1	☒	Method for storing board revision	713/2
40	US 6405302 B1	☒	Microcomputer	712/35
41	US 6338134 B1	☒	Method and system in a superscalar data processing system for the efficient processing of an instruction by moving only pointers to data	712/217
42	US 6332186 B1	☒	Vector register addressing	711/217
43	US 6314504 B1	☒	Multi-mode memory addressing using variable-length	711/212
44	US 6311263 B1	☒	Data processing circuits and interfaces	712/36
45	US 6304963 B1	☒	Handling exceptions occuring during processing of vector instructions	712/244
46	US 6282634 B1	☒	Apparatus and method for processing data having a mixed vector/scalar register file	712/210
47	US 6275982 B1	☒	Method and device enabling a fixed program to be developed	717/168
48	US 6269436 B1	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
49	US 6266727 B1	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/105
50	US 6247113 B1	☒	Coprocessor opcode division by data type	712/200
51	US 6233637 B1	☒	Isochronous data pipe for managing and manipulating a high-speed stream of isochronous data flowing between an application and a bus structure	710/311
52	US 6212630 B1	☒	Microprocessor for overlapping stack frame allocation with saving of subroutine data into stack area	712/242
53	US 6209080 B1	☒	Constant reconstruction processor that supports reductions in code size and processing time	712/212
54	US 6208104 B1	☒	Robot control unit	318/568.11
55	US 6205544 B1	☒	Decomposition of instructions into branch and sequential code sections	712/230
56	US 6189094 B1	☒	Recirculating register file	712/222
57	US 6189092 B1	☒	Pipeline processor capable of reducing branch hazards with small-scale circuit	712/241
58	US 6170001 B1	☒	System for transfering format data from format register to memory wherein format data indicating the distribution of single or double precision data type in the register bank	708/495
59	US 6167471 A	☒	Method of and apparatus for dispatching a processing element to a program location based on channel number of received data	710/62
60	US 6151673 A	☒	Data processor	712/243

	Document ID	U	Title	Current OR
61	US 6088786 A	☒	Method and system for coupling a stack based processor to register based functional unit	712/200
62	US 6079012 A	☒	Computer that selectively forces ordered execution of store and load operations between a CPU and a shared memory	712/216
63	US 6075942 A	☒	Encoding machine-specific optimization in generic byte code by using local variables as pseudo-registers	717/138
64	US 6014734 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
65	US 6009509 A	☒	Method and system for the temporary designation and utilization of a plurality of physical registers as a stack	712/202
66	US 5999737 A	☒	Link time optimization via dead code elimination, code motion, code partitioning, code grouping, loop analysis with code motion, loop invariant analysis and active variable to register analysis	717/162
67	US 5991785 A	☒	Determining an extremum value and its index in an array using a dual-accumulation processor	708/207
68	US 5987596 A	☒	Register rename stack for a microprocessor	712/217
69	US 5987495 A	☒	Method and apparatus for fully restoring a program context following an interrupt	718/108
70	US 5983018 A	☒	Debug interrupt-handling microcomputer	717/127
71	US 5982294 A	☒	Paging receiver which performs data communication protocol analysis through execution of control program	340/7.44
72	US 5978904 A	☒	Data processor	712/233
73	US 5966539 A	☒	Link time optimization with translation to intermediate program and following optimization techniques including program analysis code motion live variable set generation order analysis, dead code elimination and load invariant analysis	717/156
74	US 5960210 A	☒	Nested-loop-specialized circuitry for repeatedly performed arithmetic operations in digital signal processor and method thereof	712/1
75	US 5960203 A	☒	Assembler device and its assembling method for use in a microcomputer or other computer system	717/151
76	US 5960197 A	☒	Compiler dispatch function for object-oriented C	717/116
77	US 5944800 A	☒	Direct memory access unit having a definable plurality of transfer channels	710/23
78	US 5937188 A	☒	Instruction creation device	717/104
79	US 5928357 A	☒	Circuitry and method for performing branching without pipeline delay	712/235
80	US 5928321 A	☒	Task and stack manager for digital video decoding	718/1
81	US 5924114 A	☒	Circular buffer with two different step sizes	711/110
82	US 5907716 A	☒	Fifo buffer capable of partially erasing data set held therein	710/54

	Document ID	U	Title	Current OR
83	US 5903749 A	☒	Method and apparatus for implementing check instructions that allow for the reuse of memory conflict information if no memory conflict occurs	712/226
84	US 5881278 A	☒	Return address prediction system which adjusts the contents of return stack storage to enable continued prediction after a mispredicted branch	712/242
85	US 5881260 A	☒	Method and apparatus for sequencing and decoding variable length instructions with an instruction boundary marker within each instruction	712/210
86	US 5867726 A	☒	Microcomputer	712/32
87	US 5864707 A	☒	Superscalar microprocessor configured to predict return addresses from a return stack storage	712/23
88	US 5864706 A	☒	Digital signal processing apparatus and information processing system	712/35
89	US 5850543 A	☒	Microprocessor with speculative instruction pipelining storing a speculative register value within branch target buffer for use in speculatively executing instructions after a return	712/238
90	US 5797025 A	☒	Processor architecture supporting speculative, out of order execution of instructions including multiple speculative branching	712/23
91	US 5771366 A	☒	Method and system for interchanging operands during complex instruction execution in a data processing system	712/217
92	US 5754811 A	☒	Instruction dispatch queue for improved instruction cache to queue timing	712/214
93	US 5729723 A	☒	Data processing unit	712/222
94	US 5717946 A	☒	Data processor	712/225
95	US 5708841 A	☒	Processor architecture providing speculative, out of order execution of instructions	712/23
96	US 5706465 A	☒	Computers having cache memory	711/123
97	US 5701449 A	☒	Data processor	712/239
98	US 5687349 A	☒	Data processor with branch target address cache and subroutine return address cache and method of operation	711/137
99	US 5687336 A	☒	Stack push/pop tracking and pairing in a pipelined processor	712/202
100	US 5684672 A	☒	Programmable servo burst sequencer for a disk drive	711/4
101	US 5669012 A	☒	Data processor and control circuit for inserting/extracting data to/from an optional byte position of a register	712/1
102	US 5664135 A	☒	Apparatus and method for reducing delays due to branches	712/201
103	US 5640583 A	☒	Programmable servo burst decoder	713/600
104	US 5640538 A	☒	Programmable timing mark sequencer for a disk drive	703/23

	Document ID	U	Title	Current OR
105	US 5615386 A	☒	Computer architecture for reducing delays due to branch instructions	712/238
106	US 5606682 A	☒	Data processor with branch target address cache and subroutine return address cache and method of operation	711/204
107	US 5581775 A	☒	History buffer system	712/240
108	US 5581719 A	☒	Multiple block line prediction	712/207
109	US 5550994 A	☒	Condition decision circuit for a microcomputer	712/236
110	US 5542060 A	☒	Data processor including a decoding unit for decomposing a multifunctional data transfer instruction into a plurality of control codes	712/208
111	US 5526498 A	☒	Pipeline processor, with a return address stack and two stack pointers, for storing pre-return processed addresses	712/239
112	US 5504901 A	☒	Position independent code location system	717/144
113	US 5499379 A	☒	Input/output execution apparatus for a plural-OS run system	710/40
114	US 5481684 A	☒	Emulating operating system calls in an alternate instruction set using a modified code segment descriptor	712/212
115	US 5471593 A	☒	Computer processor with an efficient means of executing many instructions simultaneously	712/235
116	US 5469572 A	☒	Post compile optimizer for linkable object code	717/152
117	US 5450610 A	☒	RISC system capable of performing calls and returns without advancing or restoring window pointers	712/41
118	US 5414864 A	☒	Method for selectively saving/restoring first registers and bypassing second registers in register units based on individual lock/unlock status thereof	712/228
119	US 5404470 A	☒	Information processing apparatus for processing instructions by out-of-order execution	712/217
120	US 5381547 A	☒	Method for dynamically linking definable program elements of an interactive data processing system	719/331
121	US 5359730 A	☒	Method of operating a data processing system having a dynamic software update facility	717/169
122	US 5355459 A	☒	Pipeline processor, with return address stack storing only pre-return processed addresses for judging validity and correction of unprocessed address	712/242
123	US 5345570 A	☒	Microprogram control circuit	712/248
124	US 5335334 A	☒	Data processing apparatus having a real memory region with a corresponding fixed memory protection key value and method for allocating memories therefor	711/164
125	US 5321825 A	☒	Processing system with lock spaces for providing critical section access	711/163
126	US 5321822 A	☒	Information processing system with addressing exception	711/214
127	US 5307502 A	☒	Data processing system having multiple register management for call and return operations	712/41

	Document ID	U	Title	Current OR
128	US 5301289 A	☒	Cache device for supplying a fixed word length of a variable instruction code and instruction fetch device	711/213
129	US 5301231 A	☒	User defined function facility	713/191
130	US 5297239 A	☒	Compile type knowledge processing tool, a high-speed inference method therefor and a system using the tool	706/59
131	US 5293624 A	☒	Data chaining mechanism for SCSI devices	710/5
132	US 5226132 A	☒	Multiple virtual addressing using/comparing translation pairs of addresses comprising a space address and an origin address (STO) while using space registers as storage devices for a data processing system	711/209
133	US 5214786 A	☒	RISC system performing calls and returns without saving or restoring window pointers and delaying saving until multi-register areas are filled	712/41
134	US 5193205 A	☒	Pipeline processor, with return address stack storing only pre-return processed address for judging validity and correction of unprocessed address	712/239
135	US 5048439 A	☒	Computerized sewing machine	112/458
136	US 5036458 A	☒	Information processor executing interruption program without saving contents of program counter	712/244
137	US 5031096 A	☒	Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor	711/169
138	US 4992932 A	☒	Data processing device with data buffer control	712/237
139	US 4972315 A	☒	Data flow machine	712/201
140	US 4850204 A	☒	Adaptive defrost system with ambient condition change detector	62/234
141	US 4847759 A	☒	Register selection mechanism and organization of an instruction prefetch buffer	710/53
142	US 4807120 A	☒	Temporal garbage collector with indirection cells	707/206
143	US 4807115 A	☒	Instruction issuing mechanism for processors with multiple functional units	712/215
144	US 4799151 A	☒	Microprogram control circuit	712/243
145	US 4562538 A	☒	Microprocessor having decision pointer to process restore position	714/15
146	US 4479194 A	☒	System and method for reading marks on a document	235/386
147	US 4443865 A	☒	Processor module for a programmable controller	712/242
148	US 4412471 A	☒	Synchronization system for an electronic musical instrument having plural automatic play features	84/713
149	US 4399507 A	☒	Instruction address stack in the data memory of an instruction-pipelined processor	712/219

	Document ID	U	Title	Current OR
150	US 4338663 A	☒	Calling instructions for a data processing system	712/228
151	US 4297029 A	☒	Apparatus and method for diagnostic entry	355/133
152	US 4241399 A	☒	Calling instructions for a data processing system	712/228
153	US 4241397 A	☒	Central processor unit for executing instructions with a special operand specifier of indeterminate length	711/220
154	US 4241396 A	☒	Tagged pointer handling apparatus	711/154
155	US 4240142 A	☒	Data processing apparatus providing autoincrementing of memory pointer registers	712/42
156	US 4236206 A	☒	Central processor unit for executing instructions of variable length	712/204
157	US 4104721 A	☒	Hierarchical security mechanism for dynamically assigning security levels to object programs	711/164
158	US 4090237 A	☒	Processor circuit	711/212
159	US 4079455 A	☒	Microprocessor architecture	712/42
160	US 4057850 A	☒	Processing link control device for a data processing system processing data by executing a main routine and a sub-routine	712/242
161	US 4028670 A	☒	Fetch instruction for operand address calculation	712/209
162	US 3984670 A	☒	Expandable digital arithmetic logic register stack	708/190
163	US 3943494 A	☒	Distributed execution processor	712/226
164	US 3754218 A	☒	DATA HANDLING SYSTEM WITH RELOCATION CAPABILITY COMPRISING OPERAND REGISTERS ADAPTED THEREFOR	711/220

	L #	Hits	Search Text	DBs
1	L1	59740	(bit field tag flag cod$3 encod$3) near10 instruction	USPAT; US-PGPUB
2	L12	24001	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer locat$3 position) near10 (call$3 different separate$3 first second subroutine above below minus plus subtract$3 add$3))	USPAT; US-PGPUB
3	L13	399	1 near99 12	USPAT; US-PGPUB
4	L14	11017	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer) near10 (call$3 different separate$3 second subroutine above below minus plus subtract$3 add$3))	USPAT; US-PGPUB
5	L15	164	1 near99 14	USPAT; US-PGPUB
6	L16	235	13 not 15	USPAT; US-PGPUB
7	L17	19133	(bit field tag flag cod$3 encod$3) near10 instruction	EPO; JPO; DERWENT; IBM_TDB
8	L20	4403	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer locat$3 position) near10 (call$3 different separate$3 first second subroutine above below minus plus subtract$3 add$3 allocat$3))	EPO; JPO; DERWENT; IBM_TDB
9	L21	97	17 and 20	EPO; JPO; DERWENT; IBM_TDB
10	L22	24825	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer locat$3 position) near10 (call$3 different separate$3 first second subroutine above below minus plus subtract$3 add$3 allocat$3))	USPAT; US-PGPUB
11	L24	18	1 near99 22 not 13	USPAT; US-PGPUB
12	L25	29280	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer locat$3 position) near20 (call$3 different separate$3 first second subroutine above below minus plus subtract$3 add$3 allocat$3))	USPAT; US-PGPUB
13	L26	129	1 near99 25 not 13	USPAT; US-PGPUB
14	L27	5372	(register argument variable static parameter value) near10 (sav$3 stor$3) near20 ((stack frame region space area pointer locat$3 position) near20 (call$3 different separate$3 first second subroutine above below minus plus subtract$3 add$3 allocat$3))	EPO; JPO; DERWENT; IBM_TDB
15	L28	20	17 and 27 not 21	EPO; JPO; DERWENT; IBM_TDB

	Document ID	U	Title	Current OR
1	US 20010 02197 1 A1	☐	SYSTEM FOR EXECUTING INSTRUCTIONS HAVING FLAG FOR INDICATING DIRECT OR INDIRECT SPECIFICATION OF A LENGTH OF OPERAND DATA	712/215
2	US 64387 45 B1	☒	Program conversion apparatus	717/137
3	US 64347 43 B1	☒	Method and apparatus for allocating stack slots	717/157
4	US 63493 79 B1	☒	System for executing instructions having flag for indicating direct or indirect specification of a length of operand data	712/210
5	US 61890 89 B1	☒	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/218
6	US 61890 87 B1	☒	Superscalar instruction decoder including an instruction queue	712/208
7	US 61263 28 A	☒	Controlled execution of partitioned code	717/114
8	US 59833 42 A	☒	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
9	US 59037 40 A	☒	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/217
10	US 57969 74 A	☒	Microcode patching apparatus and method	712/211
11	US 57969 73 A	☒	Method and apparatus for decoding one or more complex instructions into concurrently dispatched simple instructions	712/208
12	US 57297 48 A	☒	Call template builder and method	717/137
13	US 55985 60 A	☒	Tracking condition codes in translation code for different machine architectures	717/159
14	US 54189 58 A	☒	Register allocation by decomposing, re-connecting and coloring hierarchical program regions	717/156
15	US 53392 38 A	☒	Register usage tracking in translating code for different machine architectures by forward and reverse tracing through the program flow graph	717/159
16	US 53074 92 A	☒	Mapping assembly language argument list references in translating code for different machine architectures	717/159
17	US 53013 25 A	☒	Use of stack depth to identify architechture and calling standard dependencies in machine code	717/159
18	US 44868 31 A	☒	Multi-programming data processing system process suspension	718/100

	Document ID	U	Title	Current OR
1	JP 2000029865 A	☐	DATA PROCESSOR	
2	JP 10312281 A	☒	METHOD AND SYSTEM FOR PROCESSING INSTRUCTION	
3	JP 07072908 A	☒	PROGRAMMABLE CONTROLLER	
4	JP 05298099 A	☒	CONTINUOUS PROCESSING METHOD FOR PLURAL PROGRAMS AND CENTRAL PROCESSING UNIT USING THE SAME	
5	JP 01260537 A	☒	EQUIPMENT CONTROL PROCESSOR CIRCUIT	
6	JP 01116828 A	☒	DATA ARITHMETIC PROCESSING DEVICE	
7	JP 01003750 A	☒	PROGRAM TRACING SYSTEM	
8	JP 63247834 A	☒	PROCESSING METHOD FOR PSEUDO INSTRUCTION OF FLOATING POINT FUNCTION	
9	JP 61161545 A	☒	DATA PROCESSING SYSTEM	
10	EP 634717 A2	☒	Data processing unit.	
11	EP 215992 A1	☒	Method for storing the control code of a processor allowing effective code modification and addressing circuit therefor.	
12	KR 2001053729 A	☒	Signal recording method in data service in mobile communication area	
13	US 5740093 A	☒	Computer with quadruple precision compatibility - includes 128-bit register file and 128-bit floating point load and store and software emulator which perform quad precision calculations on data stored in memory	
14	US 5500948 A	☒	Instruction pointer translation method for accessing on-chip instruction cache - by comparing upper order bit of logical address with stored values in first and second logical register	
15	US 5437011 A	☒	Graphics computer system - has CPUs contg. 1st ALUs including base register and offset register, and graphics hardware contg. 2nd ALUs for processing data from graphics memory circuits in parallel with 1st ALUs processing addresses of data in graphics memory circuits	
16	GB 2239334 A	☒	Computer system employing object-oriented memory protection - provides communication between execution environment using supervisor stack pointer and procedure entry type field	
17	US 4751703 A	☒	Storing control code of processor allowing effective code modification - using addressing circuit to fetch instructions which are stored in RAM instead of RAM memory	
18	EP 215992 A	☒	Method for storing the control code of a processor - allowing effective code modification and addressing circuit therefor	
19	EP 170398 A	☒	Data processor with program scanner - scans sequence of incoming codes and employs RAMs to detect various types of syllables in code	
20	EP 407035 A	☒	Enhancement of 370 type data processor - reduces overhead incurred by multiple users by permitting program in one address space to obtain access to data in another address space	

	Document ID	U	Title	Current OR
1	US 20040 06468 3 A1	☐	System and method for conditionally executing an instruction dependent on a previously existing condition	712/226
2	US 20040 03102 2 A1	☒	Information processing device for multiple instruction sets with reconfigurable mechanism	717/139
3	US 20040 01988 4 A1	☒	Eliminating cold register store/restores within hot function prolog/epilogs	717/154
4	US 20040 01570 7 A1	☒	Control system for protecting external program codes	713/189
5	US 20030 13577 9 A1	☒	Microprocessor	713/600
6	US 20030 10579 3 A1	☒	Long instruction word controlling plural independent processor operations	708/625
7	US 20030 07911 4 A1	☒	Processor, compiling apparatus, and compile program recorded on a recording medium	712/213
8	US 20010 05414 0 A1	☒	MICROPROCESSOR INCLUDING AN EFFICIENT IMPLEMENTATION OF EXTREME VALUE INSTRUCTIONS	712/223
9	US 20010 02197 1 A1	☐	SYSTEM FOR EXECUTING INSTRUCTIONS HAVING FLAG FOR INDICATING DIRECT OR INDIRECT SPECIFICATION OF A LENGTH OF OPERAND DATA	712/215
10	US 66437 75 B1	☒	Use of code obfuscation to inhibit generation of non-use-restricted versions of copy protected software applications	713/190
11	US 65570 98 B2	☒	Microprocessor including an efficient implementation of extreme value instructions	712/223
12	US 64906 73 B1	☒	Processor, compiling apparatus, and compile program recorded on a recording medium	712/213
13	US 64877 13 B1	☒	Software development system that presents a logical view of project components, facilitates their selection, and signals missing links prior to compilation	717/105
14	US 64809 59 B1	☒	Software system and associated methods for controlling the use of computer programs	713/189
15	US 64808 18 B1	☒	Debugging techniques in a multithreaded environment	703/26
16	US 64497 12 B1	☒	Emulating execution of smaller fixed-length branch/delay slot instructions with a sequence of larger fixed-length instructions	712/227
17	US 64387 45 B1	☒	Program conversion apparatus	717/137
18	US 64347 43 B1	☒	Method and apparatus for allocating stack slots	717/157
19	US 63670 05 B1	☒	System and method for synchronizing a register stack engine (RSE) and backing memory image with a processor's execution of instructions during a state saving context switch	712/228
20	US 63493 79 B1	☒	System for executing instructions having flag for indicating direct or indirect specification of a length of operand data	712/210

	Document ID	U	Title	Current OR
21	US 6334189 B1	☒	Use of pseudocode to protect software from unauthorized use	713/200
22	US 6314513 B1	☒	Method and apparatus for transferring data between a register stack and a memory resource	712/228
23	US 6298440 B1	☒	Method and system for providing multiple entry point code resources	713/1
24	US 6292844 B1	☒	Media storage device with embedded data filter for dynamically processing data during read and write operations	710/5
25	US 6219783 B1	☒	Method and apparatus for executing a flush RS instruction to synchronize a register stack with instructions executed by a processor	712/228
26	US 6189089 B1	☒	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/218
27	US 6189087 B1	☒	Superscalar instruction decoder including an instruction queue	712/208
28	US 6141794 A	☒	System and method for synchronizing access to shared variables in a virtual machine in a digital computer system	717/118
29	US 6126328 A	☒	Controlled execution of partitioned code	717/114
30	US 6115777 A	☒	LOADRS instruction and asynchronous context switch	710/260
31	US 6112292 A	☒	Code sequence for asynchronous backing store switch utilizing both the cover and LOADRS instructions	712/200
32	US 6075937 A	☒	Preprocessing of stored target routines for controlling emulation of incompatible instructions on a target processor and utilizing target processor feedback for controlling non-sequential incompatible instruction emulation	703/23
33	US 6065114 A	☒	Cover instruction and asynchronous backing store switch	712/228
34	US 6029244 A	☒	Microprocessor including an efficient implementation of extreme value instructions	712/223
35	US 6016544 A	☒	Apparatus and method for tracking changes in address size and for different size retranslate second instruction with an indicator from address size	712/234
36	US 6012141 A	☒	Apparatus for detecting and executing traps in a superscalar processor	712/244
37	US 5983342 A	☒	Superscalar microprocessor employing a future file for storing results into multiportion registers	712/218
38	US 5974543 A	☒	Apparatus and method for performing subroutine call and return operations	712/240
39	US 5974524 A	☒	Method and apparatus for reducing the number of rename registers in a processor supporting out-of-order execution	712/23
40	US 5944811 A	☒	Superscalar processor with parallel issue and execution device having forward map of operand and instruction dependencies	712/23
41	US 5907500 A	☒	Motion compensation adder for decoding/decompressing compressed moving pictures	708/700
42	US 5903740 A	☒	Apparatus and method for retiring instructions in excess of the number of accessible write ports	712/217

	Document ID	U	Title	Current OR
43	US 5870701 A	☒	Control signal processing method and apparatus having natural language interfacing capabilities	704/9
44	US 5852726 A	☒	Method and apparatus for executing two types of instructions that specify registers of a shared logical register file in a stack and a non-stack referenced manner	712/200
45	US 5815646 A	☒	Decompression processor for video applications	345/502
46	US 5809174 A	☒	Decompression processor for video applications	382/236
47	US 5802219 A	☒	Methods and apparatus for table lookup transformation of digital images	382/276
48	US 5796974 A	☒	Microcode patching apparatus and method	712/211
49	US 5796973 A	☒	Method and apparatus for decoding one or more complex instructions into concurrently dispatched simple instructions	712/208
50	US 5764507 A	☒	Programmable controller with personal computerized ladder diagram	700/18
51	US 5740093 A	☒	128-bit register file and 128-bit floating point load and store for quadruple precision compatibility	708/513
52	US 5729748 A	☒	Call template builder and method	717/137
53	US 5729556 A	☒	System decoder circuit with temporary bit storage and method of operation	714/747
54	US 5692170 A	☒	Apparatus for detecting and executing traps in a superscalar processor	712/244
55	US 5659721 A	☒	Processor structure and method for checkpointing instructions to maintain precise state	712/228
56	US 5657454 A	☒	Audio decoder circuit and method of operation	375/242
57	US 5608888 A	☒	Method and apparatus for mapping data of a 2-dimensional space from a linearly addressed memory system	711/202
58	US 5598560 A	☒	Tracking condition codes in translation code for different machine architectures	717/159
59	US 5598483 A	☒	MPEG video decompression processor	382/232
60	US 5596734 A	☒	Method and apparatus for programming embedded memories of a variety of integrated circuits using the IEEE test access port	710/5
61	US 5594437 A	☒	Circuit and method of unpacking a serial bitstream	341/67
62	US 5568646 A	☒	Multiple instruction set mapping	712/209
63	US 5566303 A	☒	Microcomputer with multiple CPU'S on a single chip with provision for testing and emulation of sub CPU's	710/100
64	US 5517664 A	☒	RISC system with instructions which include register area and displacement portions for accessing data stored in registers during processing	712/41
65	US 5497459 A	☒	System for testing instruction queue circuit and central processing unit having the system	714/30

	Document ID	U	Title	Current OR
66	US 5437043 A	☒	Information processing apparatus having a register file used interchangeably both as scalar registers of register windows and as vector registers	712/1
67	US 5418958 A	☒	Register allocation by decomposing, re-connecting and coloring hierarchical program regions	717/156
68	US 5404471 A	☒	Method and apparatus for switching address generation modes in CPU having plural address generation modes	712/207
69	US 5386566 A	☒	Inter-processor communication method for transmitting data and processor dependent information predetermined for a receiving process of another processor	719/310
70	US 5379356 A	☒	Decompression processor for video applications	382/233
71	US 5339238 A	☒	Register usage tracking in translating code for different machine architectures by forward and reverse tracing through the program flow graph	717/159
72	US 5307492 A	☒	Mapping assembly language argument list references in translating code for different machine architectures	717/159
73	US 5301325 A	☒	Use of stack depth to identify architechture and calling standard dependencies in machine code	717/159
74	US 5241679 A	☒	Data processor for executing data saving and restoration register and data saving stack with corresponding stack storage for each register	710/260
75	US 5237666 A	☒	Apparatus using address of a predetermined preceding instruction and target instruction address stored in history table to prefetch target instruction	712/240
76	US 5201056 A	☒	RISC microprocessor architecture with multi-bit tag extended instructions for selectively attaching tag from either instruction or input data to arithmetic operation output	712/41
77	US 5132898 A	☒	System for processing data having different formats	712/210
78	US 5043918 A	☒	Multiple bus image controller structure for color page printers	358/1.16
79	US 5036460 A	☒	Microprocessor having miswriting preventing function	711/103
80	US 4975828 A	☒	Multi-channel data communications controller	710/11
81	US 4947411 A	☒	Programmable clock frequency divider	377/47
82	US 4782443 A	☒	Main storage control system for virtual computing function system with plural address modes in main storage access operations	718/100
83	US 4755962 A	☒	Microprocessor having multiplication circuitry implementing a modified Booth algorithm	708/628
84	US 4713750 A	☒	Microprocessor with compact mapped programmable logic array	712/32
85	US 4611286 A	☒	Cash accounting system	705/22
86	US RE31864 E	☒	Self-test feature for appliance or electronic systems operated by microprocessor	714/36
87	US 4491912 A	☒	Data processing system with improved microsubroutine facility	712/243
88	US 4486831 A	☒	Multi-programming data processing system process suspension	718/100

	Document ID	U	Title	Current OR
89	US 4439828 A	☒	Instruction substitution mechanism in an instruction handling unit of a data processing system	712/226
90	US 4306232 A	☒	Digital joystick control interface system for video games and the like	345/161
91	US 4258429 A	☒	Multiphase clocking for MOS electronic calculator or digital processor chip	712/32
92	US 4223381 A	☒	Lookahead memory address control system	712/207
93	US 4180805 A	☒	System for displaying character and graphic information on a color video display with unique multiple memory arrangement	345/161
94	US 4179736 A	☒	Microprogrammed computer control unit capable of efficiently executing a large repertoire of instructions for a high performance data processing unit	712/232
95	US 4161726 A	☒	Digital joystick control	341/9
96	US 4158432 A	☒	Control of self-test feature for appliances or electronic equipment operated by microprocessor	714/46
97	US 4158431 A	☒	Self-test feature for appliances or electronic systems operated by microprocessor	714/46
98	US 4156278 A	☒	Multiple control store microprogrammable control unit including multiple function register control field	712/248
99	US 4148014 A	☒	System with joystick to control velocity vector of a display cursor	345/161
100	US 4142180 A	☒	Digital joystick control interface system for video games and the like	345/161
101	US 4125897 A	☒	High speed pulse interpolator	708/102
102	US 4124893 A	☒	Microword address branching bit arrangement	712/230
103	US 4118773 A	☒	Microprogram memory bank addressing system	711/215
104	US 4110810 A	☒	Variable field length addressing system having data byte interchange	712/243
105	US 4107774 A	☒	Microprogram splatter return apparatus	712/231
106	US 4087857 A	☒	ROM-initializing apparatus	712/231
107	US 4054945 A	☒	Electronic computer capable of searching a queue in response to a single instruction	712/227
108	US 4042914 A	☒	Microprogrammed control of foreign processor control functions	710/23
109	US 4037090 A	☒	Multiphase clocking for MOS	708/130
110	US 4032913 A	☒	Coding equipment providing compressed code	341/138
111	US 4024386 A	☒	Electronic calculator or digital processor chip having test mode of operation	714/718

	Document ID	U	Title	Current OR
112	US 4021781 A	☒	Virtual ground read-only-memory for electronic calculator or digital processor	711/211
113	US 4021656 A	☒	Data input for electronic calculator or digital processor chip	708/139
114	US 4014013 A	☒	Direct drive display system for MOS integrated circuits using segment scanning	708/160
115	US 4014012 A	☒	Segment scanning method for calculator display system	345/46
116	US 4012601 A	☒	Automatic pushbutton dial assembly for a subscriber telephone	379/357.04
117	US 4012600 A	☒	Automatic pushbutton dial system for a subscriber telephone	379/357.04
118	US 4011414 A	☒	Automatic dial system for a subscriber telephone	379/357.05
119	US 3991306 A	☒	Electronic calculator or digital processor chip with separately controllable digit and segment outputs	708/168
120	US 3991305 A	☒	Electronic calculator or digital processor chip with multiple code combinations of display and keyboard scan outputs	708/168
121	US 3989939 A	☒	Electronic calculator or digital processor chip with combined functions for constant, keyboard and control bit	708/190
122	US 3988604 A	☒	Electronic calculator or digital processor chip having multiple function arithmetic unit output	708/190
123	US 3972023 A	☒	I/O data transfer control system	710/1
124	US 3969704 A	☒	Word transformation apparatus for digital information processing	712/204
125	US 3938104 A	☒	System for modifying a logic controller instruction set	711/100
126	US 3702007 A	☒	TABLE DRIVEN PROGRAM	712/234
127	US 3651485 A	☒	HOLOGRAPHIC DATA PROCESSING SYSTEM	700/90
128	US 3648227 A	☒	CORRECTING SEISMIC TRACES FOR STATIC CORRECTIONS AND NORMAL MOVEOUT	367/53
129	US 3618045 A	☒	MANAGEMENT CONTROL SUBSYSTEM FOR MULTIPROGRAMMED DATA PROCESSING SYSTEM	712/233